A 1.9GHz Variable Gain Linear Power Amplifier MMIC for PHS Using Novel Cascaded MESFETs

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Abstract

A GaAs power amplifier MMIC for 1.9GHz Japanese digital cordless phone has been developed using novel cascaded MESFETs. The MMIC exhibits a gain of 32dB, a power added efficiency of 37% at P-1dB of 23.6dBm, -64dBc adjacent channel leakage power (ACP) at 600KHz offset with 21dBm output, and an operating voltage of 3V. In addition, the ACP of less than -57dBc is obtained at gain control of 0dB to -14dB remaining an output power of 21dBm.

Introduction

In the market of Japanese digital cordless phone, so called PHS(Personal Handy phone System) is rapidly expanding in recent years. According to spread of the market, the demand for smaller size and lower dissipation power of hand-held terminal is increasing[1]. For the use of handy phone sets, the power amplifier in transmitters needs to meet many requirements such as 1)small package size, 2)low current and low voltage operation, 3)exception of external matching circuits and 4)low cost, while satisfying desired performances[2],[3]. This paper reports on the development of GaAs linear power amplifier MMIC for PHS handy phone sets. The MMIC features small package size, inclusion of all matching circuits, good adjacent channel leakage power performance with low dissipation power and high gain.

Besides above characteristics, the transmitter amplifier is often required to have gain control capability according to the input level. The most outstanding feature of this amplifier is the incorporation of novel cascaded FETs in 1st and 2nd stage for requirement of maintaining low adjacent channel leakage power under gain control.

Furthermore, in handy phone sets the gate voltage has to be supplied by negative voltage generator ICs, then large gate leakage current induces a serious problem of spurious noise generated in negative voltage generator ICs. The gate leakage current of the amplifier at 21dBm output is very small, which means the amplifier is very attractive when negative gate voltage is supplied by negative voltage generator ICs.

New type of cascaded FET

Conventional FET gain control amplifiers use dual gate FETs which consist of cascaded configuration of a common source FET followed by a common gate FET as shown in Figure 1[4],[5]. The dual gate FET is inferior to the single gate FET with the same gate size as for output power performance. In addition, dual gate FET gain control

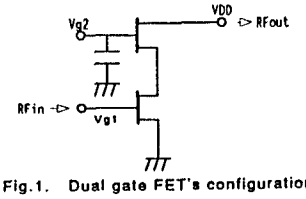

Fig.1. Dual gate FET's configuration.

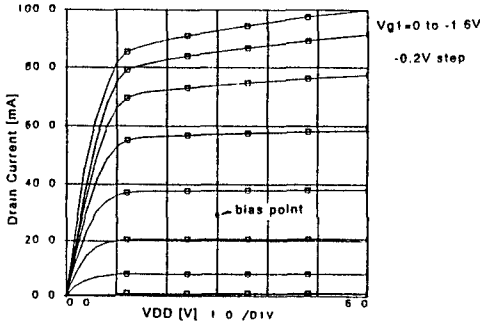

Fig 2. Predicted *ID-VD* characteristics of conventional dual gate FET(*Wg*=800um, *Vth*=-1.6V).

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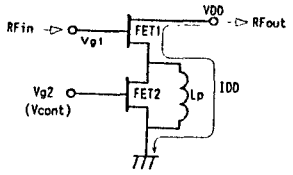
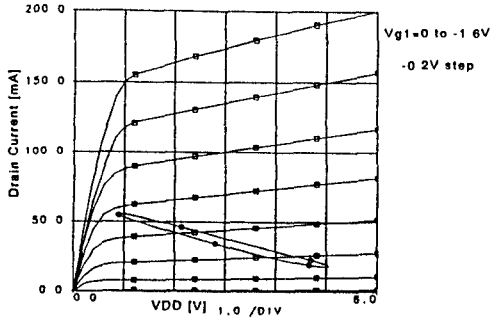
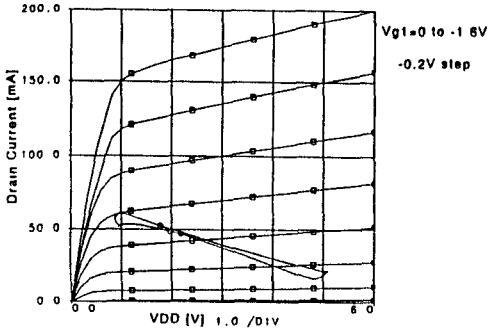


Fig 3. Novel cascaded FET's configuration.



(a) at *Vg2*=0V



(b) at *Vg2*=-1.0V

Fig.4. Predicted loaded line of the novel cascaded FET(*Wg*=800um) at Pout=15dBm, *VDD*=3V.

amplifiers have inherently disadvantage that its saturated output power performance worsens as the gain becomes lower. This degradation is due to change of *ID-VD* characteristics of the FET as a function of the second gate voltage[6],[7]. As shown in predicted results of Figure 2, the saturated drain current of the dual gate FET becomes small as well as the transconductance *gm* at the bias point when the second gate voltage is increased.

To overcome these problems, we propose a novel cascaded FET(Stack FET configuration of two common source FETs) in which a inductor *Lp* is connected between drain and source of the common source FET as shown in Figure 3. In Figure 3, upper FET(FET1) is used as a active device for the amplifiers and lower FET(FET2) can play a role of variable resistor *Rv* by varying its gate voltage *Vg2*. Therefore, the new cascaded FET is equivalent to a single gate FET having variable series feedback circuit whose impedance is *Zv* in the source.

$$Zv = j\,\omega\, Rv \cdot Lp / (Rv + j\,\omega\, Lp)$$

On the other hand, since the drain current of FET1 passes through *Lp*, *ID-VD* characteristics and the bias current of FET1 is constant for any variable value of *Rv*. That results in a solution of the output power degradation for a variable gain in dual gate FETs. Figure 4 shows the predicted dynamic load lines at an output power of 15dBm for the cascaded FET with gate width of 800um and threshold voltage of -1.6V, which input and output conjugate match is applied. Figure 4-(a) displays the calculated results at *Vg2*=0V which gives maximum gain, and Figure 4-(b) shows that one at *Vg2*=-1V which provides -10dB gain suppression, respectively. It can be seen that there is no remarkable twist with the loaded line and no change for *ID-VD* characteristics at *Vg2*=-1V compared to at *Vg2*=0V. Thus, our new cascaded FET can carry out gain control with an available saturated output power remaining fixed.

Predicted results of Figure 2 and 4 are produced by applying Curtice cubic model to each single gate FET of Figure 1 and Figure 3.

Three-stage power amplifier

A schematic diagram of the developed three-stage power amplifier MMIC is shown in Figure 5. In order to realize an output power and an adjacent channel leakage power(ACP) performance required in the systems with variable gain, the cascaded FETs mentioned above are incorporated in 1st and 2nd stages. The gain control is achieved by varying gain control voltage *Vcont* supplied to each *Vg2* port of 1st and 2nd cascaded FETs. *Wg* of 1st ,2nd and 3rd FETs are 300um, 800um and 3200um, respectively. To reduce die size, a lumped element C-L-C input matching network and also lumped L-C interstage matching networks are applied. The output matching network is designed to achieve high power added efficiency(PAE) and low ACP at an output power of 21dBm. The optimum load impedance is 12.3 + j6.7 (Ω). All of matching networks are constructed on chips. Inductance *Lp1* and *Lp2* are determined to get more than 20dB gain control range for the amplifier.

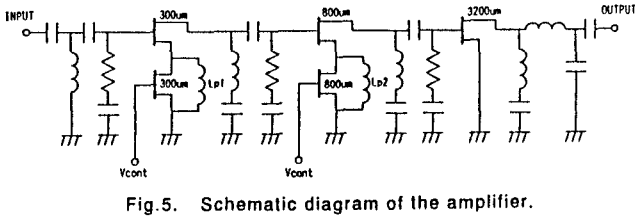
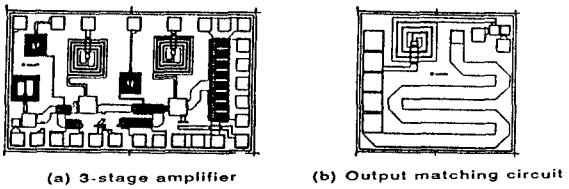


Fig.5. Schematic diagram of the amplifier.



(a) 3-stage amplifier (b) Output matching circuit

Fig.6. Chip layout of the MMIC.

Fabrication

The wafers are manufactured using a standard ion implant recess gate MESFET process with a nominal 0.5um gate length, 20GHz *ft*, threshold voltage of -1.6V. *Lgs* of 0.5um and *Lgd* of 0.8um are chosen to achieve low kee- voltage of 1.0V and high gate-drain breakdown voltage of 14V. A buried *p*-layer contributes to reduction of the gate leakage current.

The noteworthy feature on fabrication of the MMIC is that the amplifier consists of two chips: a three-stage amplifier chip and an output matching circuit chip, which are composed of GaAs substrates. The output matching circuit chip is fabricated by use of wafer process for passive circuits employing 3um-Au-thickness. These chips are mounted on the leadframe of SSOP14 package designed the characteristic impedance of RF input and output leads to be 50 Ω, and are connected each other using five bond wire to reduce the effect of parasitic inductance. The power dissipation capability of the package is 600mW.

The chip layouts are shown in Figure 6. Die size of the three-stage amplifier is 1.1x1.85mm, and the output matching circuit is 1.1x1.2mm.

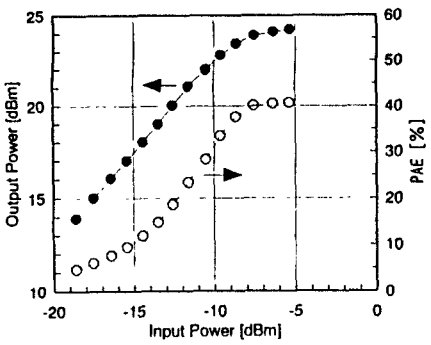


Fig.7. Output power, PAE performance at *VDD*=3V, *Iidle*=170mA.

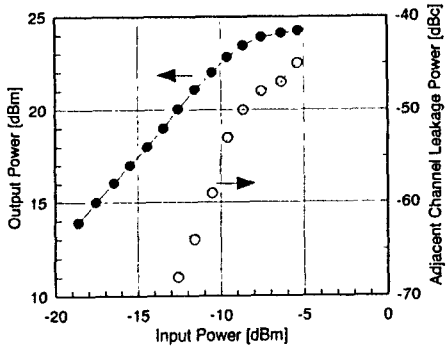


Fig.8. Output power, ACP performance at *VDD*=3V, *Iidle*=170mA.

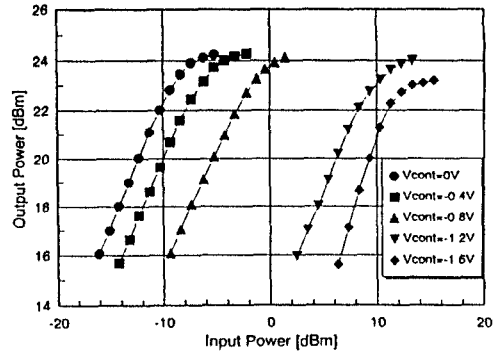


Fig.9. Output power performance as a function of *Vcont* at *VDD*=3V, *Iidle*=170mA.

Results

The MMIC is soldered to a 0.2mm thickness FR4 microstrip board with coaxial connectors in RF input and output. Figure 7,8 shows the measured output power, PAE and ACP at *VDD*=3.0V and *Vcont*=0V. The idle current *Iidle* is 170mA. The 1-dB gain compression power of 23.6dB at 37% PAE is achieved. The ACP at 600KHz offset for a 384Kbps $\pi/4$-DQPSK signal is less than -64dBc at an output power of 21dBm. Also, the ACP of less than -58dBc has been measured at *VDD*=2.7V.

Input-output power performances at five deferent *Vcont* conditions are shown in Figure 9. In the gain control range of 20dB (-1.2V<*Vcont*<0V), the saturated output power of more than 24dBm is accomplished.

Figure 10,11 and 12 demonstrate the gain control capability of the amplifier. The gain control of more than 23dB and the negligible effect on both input and output matches are achieved at several *Vcont* from 0V to -1.6V.

The gain and ACP versus *Vcont* performance at Pout of 21dBm is shown in Figure 13. As is seen, remaining Pout of 21dBm, the ACP of less than -57dBc is measured at the gain of 32dB to 18dB by changing *Vcont* from 0 to -1.0V.

Figure 14 shows the output power and gate leakage current versus input power. The amplifier also features low gate leakage current of -5uA at Pout of 21dBm.

Conclusion

A GaAs power amplifier MMIC for 1.9GHz Japanese digital cordless phone has been developed using novel cascaded MESFETs. The MMIC exhibits a gain of 32dB, a power added efficiency of 37% at P-1dB of 23.6dBm, -64dBc adjacent channel leakage power at 600KHz offset with 21dBm output, and an operating voltage of 3V. In addition, the ACP of less than -57dBc is obtained at gain control of 0dB to -14dB remaining an output power of 21dBm. Furthermore, the gate

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leakage current at 21dBm output is very small which means the amplifier is very attractive when negative gate voltage is supplied by negative voltage generator ICs.

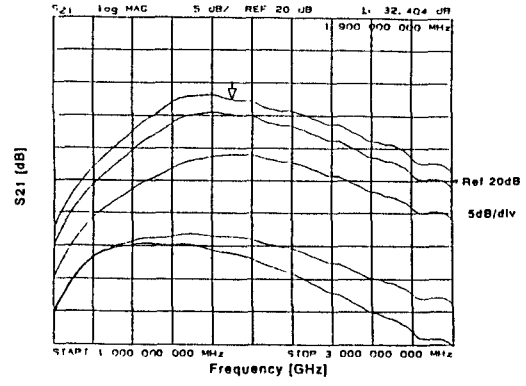

Fig.10. Gain variation performance as a function of *Vcont*(*Vcont*=0 to -1.6V, -0.4V step)at *VDD*=3V,*IDD*=170mA.

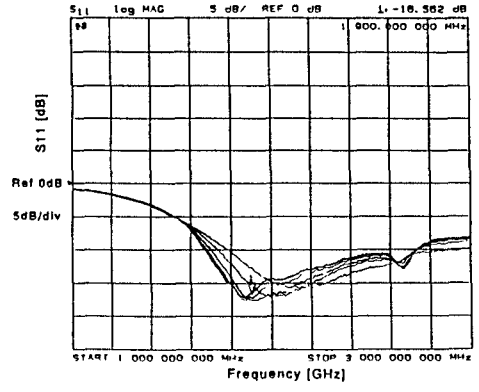

Fig.11. Input return-loss variation as a function of *Vcont*(*Vcont*=0 to -1.6V, -0.4V step)at *VDD*=3V,*IDD*=170mA.

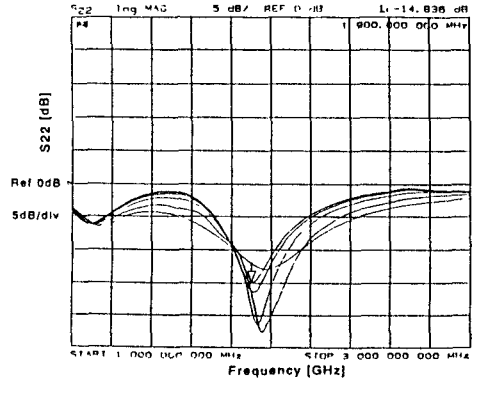

Fig.12. Output return-loss variation as a function of *Vcont*(*Vcont*=0 to -1.6V, -0.4V step) at *VDD*=3V,*IDD*=170mA.

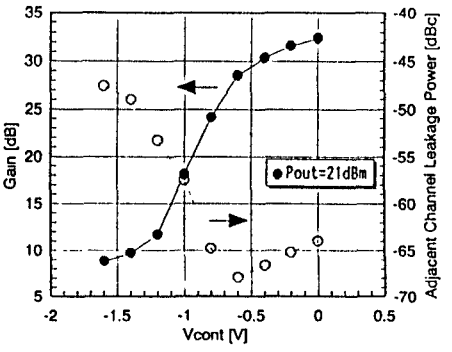

Fig.13. Gain, ACP performance as a function of *Vcont* at Pout=21dBm, *VDD*=3V, *Iidle*=170mA.

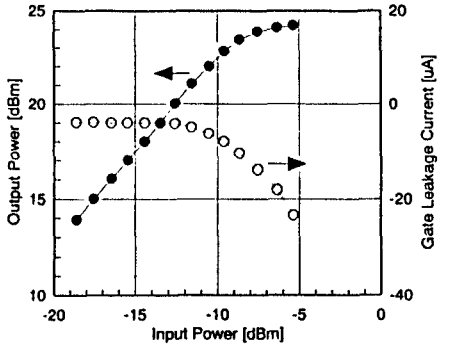

Fig.14. Output power, gate leakage current performance at *VDD*=3V, *Iidle*=170mA.

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